CLAIMS

WHAT IS CLAIMED IS:

1. A method comprising:

moving an inverting buffer from a source to a sink in a netlist if both inverting and non-inverting signals are to be sent from the source to the sink.

2. The method of claim 1, wherein the moving further comprises:

finding the inverting buffer associated with the source in the netlist;

removing the inverting buffer associated with the source; and

adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes.

3. The method of claim 2, wherein at least a first route of the plurality of routes is to send the inverting signals and at least a second route of the plurality of routes is to send the non-inverting signals.

4. The method of claim 3, further comprising:

removing the first route.

5. The method of claim 2, wherein the adding is performed prior to chip placement, timing optimizations, and routing.

6. The method of claim 2, wherein the adding is performed after chip placement and before timing optimizations and routing.

7. An apparatus comprising:

means for finding an inverting buffer associated with a source in a netlist;

means for removing the inverting buffer associated with the source; and

means for adding the inverting buffer to a sink, wherein the sink is connected to the source via a plurality of routes, and wherein at least a first route of the plurality of routes is to send inverting signals and at least a second route of the plurality of routes is to send non-inverting signals.

8. The apparatus of claim 7, further comprising:

means for removing the first route.

9. The apparatus of claim 7, wherein the means for adding is performed prior to chip placement, timing optimizations, and routing.

10. The apparatus of claim 7, wherein the means for adding is performed after chip placement and before timing optimizations and routing.

11. A signal-bearing medium encoded with instructions, wherein the instructions when executed comprise:

finding an inverting buffer associated with a source in a netlist;

removing the inverting buffer associated with the source;

adding the inverting buffer to a sink, wherein the sink is connected to the source via a plurality of routes; and

removing at least one of the plurality of routes.

12. The signal-bearing medium of claim 11, wherein the adding is performed prior to chip placement, timing optimizations, and routing.

13. The signal-bearing medium of claim 11, wherein the adding is performed after chip placement and before timing optimizations and routing.

14. The signal-bearing medium of claim 11, wherein the source represents a source region in a floorplanned chip and the sink represents a sink region in the floorplanned chip.

15. The signal-bearing medium of claim 11, wherein the source and sink are in a chip without floorplans.

16. The signal-bearing medium of claim 11, wherein the source and sink are in a same subpartition of a chip.

17. An electronic device comprising:

a processor; and

a storage device encoded with instructions, wherein the instructions when executed on the processor comprise:

finding an inverting buffer associated with a source in a netlist,

removing the inverting buffer associated with the source,

adding the inverting buffer to a sink, wherein the sink is connected to the source via a plurality of routes, and wherein at least a first route of the plurality of routes is to send inverting signals and at least a second route of the plurality of routes is to send non-inverting signals, and

removing the first route.

18. The electronic device of claim 16, wherein the source represents a source region in a floorplanned chip and the sink represents a sink region in the floorplanned chip.

19. The electronic device of claim 16, wherein the source and sink are in a chip without floorplans.

20. The electronic device of claim 16, wherein the source and sink are in a same subpartition of a chip.